CLAIMS

1. An insulated gate field effect transistor having a gate electrode on a substrate with a gate insulating film interposed between said substrate and said gate electrode, and having a source region and a drain region formed in said substrate on both sides of said gate electrode, said insulated gate field effect transistor comprising:

a first diffusion layer of a first conduction type formed in said substrate at a position deeper than said source region and said drain region; and

a second diffusion layer of the first conduction type having a higher concentration than said first diffusion layer and formed in said substrate at a position deeper than said first diffusion layer.

2. An insulated gate field effect transistor as claimed in claim 1,

wherein a diffusion layer of a second conduction type is formed between said source region and said drain region in said substrate with a region of said substrate left on a side of said gate electrode.

3. An insulated gate field effect transistor as claimed in claim 2,

wherein said first conduction type is a P type, and

said second conduction type is an N type.

4. A method of manufacturing an insulated gate field effect transistor having a gate electrode on a substrate with a gate insulating film interposed between said substrate and said gate electrode, and having a source region and a drain region formed in said substrate on both sides of said gate electrode, said method comprising:

a step for forming in advance a first diffusion layer of a first conduction type in said substrate at a position deeper than a region where said source region and said drain region are formed in said substrate; and

a step for forming in advance a second diffusion layer of the first conduction type having a higher concentration than said first diffusion layer and formed in said substrate at a position deeper than said first diffusion layer.

5. A method of manufacturing an insulated gate field effect transistor, as claimed in claim 4, wherein a diffusion layer of an N type is formed in advance in a region between said source region and said drain region formed in said substrate with a region of said substrate left on a surface side of said substrate.

6. An image pickup device, wherein a part or all

of insulated gate field effect transistors forming an output circuit in the image pickup device and formed in a substrate comprise:

a first diffusion layer of a first conduction type formed in said substrate at a position deeper than each source region and each drain region of said insulated gate field effect transistors; and

a second diffusion layer of the first conduction type having a higher concentration than said first diffusion layer and formed in said substrate at a position deeper than said first diffusion layer.

7. A method of manufacturing an image pickup device in which a part or all of insulated gate field effect transistors form an output circuit in the image pickup device and are formed in a substrate, said method comprising:

a step for forming in advance a first diffusion layer of a first conduction type in said substrate where said insulated gate field effect transistors are formed, at a position deeper than a region where a source region and a drain region of said insulated gate field effect transistors are formed; and

a step for forming in advance a second diffusion layer of the first conduction type having a higher

concentration than said first diffusion layer in said substrate at a position deeper than said first diffusion layer.